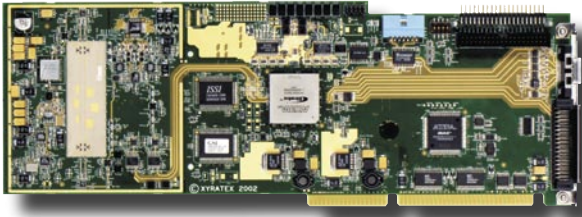


Pattern Generation for the future



Features

- Fast – 400 Mbit/sec
- Accurate – Advanced Digital PLL
- Enhanced – Head Parametrics Capability
- Flexible – Open architecture

Xyratex Pattern Generator Technology is widely used in the industry. Xyratex has doubled the performance with its latest design. This now includes support for the newest advances in optical clocking technology; continuing its commitment to maintain its position at the head of the technology curve.

Xtreme 400 includes a Pattern Generator card, a companion Channel card and software.

Xtreme 400 is integrated into the current Xyratex Electronic package. This contains a motor driver and interlocks card, power and ancillary cabling within a compact casing.



High Level Technical Specification

Clock Writer

- Programmable Clock Closure
- Programmable Closure Error to 0.75ns
- Closure Error Correction
- Clock Index Slip Detection to Ts Resolution

Enhanced Digital PLL

- Loop Filter to Control Bandwidth
- 5 Bit Phase Detector Resolution (+/- 1 T'State range)
- DPLL Resolution Ts/1024
- Configurable DPLL Update Rate Ts*4 – Ts*64

Pattern Generation

- Enhanced Maximum Ts Rate to 400Mbit/sec
- Enhanced Ts/Revolution to 4Mbit

Pattern Generator Key Features

- Pattern Frequencies to 400Mbit/sec Fs (200MHz written)
- Clock Track Advanced Digital Phase Lock Loop (ADPLL) & verify logic
- Clock Track Writer with user defined index pattern
- Multiple 4Mbit Open Architecture Pattern Buffers
- Dynamically Configurable Pattern Encoder
- Fully programmable clock writer/verifier
- Flexible open architecture for maximum configurability and ease of integration
- SRAM Based FPGA Pattern Generator Core to allow easy field upgradeability
- Bank and Staggered head writing
- Index or early pattern writing
- Optical clock capable

Channel Card Key Features

- Support for 400Mbit/sec Fs (200MHz Written Frequency)
- Support for GMR/TF Clock Preamp
- Head Parametric option provides product head measurements for drive at first point of integration
- SRAM Based FPGA core to allow easy field upgradeability



Software Key Features

- Easy to use and extend
- New Pattern Generation System
- Simple INI and script files
- Allows customers to easily re-configure for other products
- Open system allows customers to support unique requirements
- Supports customer written software modules

- Enhanced Configurable Servo Sectors up to 8196
- Reduced Electronic TTPE Contribution to < 150ps 1 sigma
- Pattern Pulse Symmetry 0.25ns at 400MHz
- Servo Frame Timing Resolution T-state
- Pattern Update (Multiple Buffers) < 1.5ms
- Write Synchronization to index (Index Write) or Next Servo Sector (Early Write)
- Maximum Pattern Buffers 6

Other Features

- Dedicated Differential High Speed Cabling for Critical Signals
- EEPROM Included to Track Card & Store Configuration Data
- AT Bus IRQ Support for End of Write Notification/Error Status
- Companion Channel Interface SPI Rate Increased 40Mbit/Sec

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